UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,064	11/21/2001	Ashley Saulsbury	188440/US	4869

66083 7590 09/18/2007

SUN MICROSYSTEMS, INC. c/o DORSEY & WHITNEY, LLP
370 SEVENTEENTH ST.
SUITE 4700
DENVER, CO 80202

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
09/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/992,064
Filing Date: November 21, 2001
Appellant(s): SAULSBURY ET AL.

Ashley Saulsbury et al.

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/02/2007 appealing from the Office action mailed 04/14/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include: (1) a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters and (2) for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters. The brief is deficient because the summary of the claimed subject matter in pages 4-5 fails to provide a concise explanation of subject matter in independent

claims along with corresponding specific citation in the original specification. Even though, the summary of the claimed subject matter in pages 4-5 addresses all independent claims 1, 8, and 18. However, it fails to address in detail the citations of each individual limitations cited in the claims.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,889,242	Sijstermans et al.	5-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sijstermans et al. (U.S. 6,889,242). In particular,

whether the cited reference by Sijsterman et al. disclose every features of independent method claims 1 and 8; and

whether the cited reference by Sijstermans et al. disclose every features of independent apparatus claim 18.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sijstermans et al. (U.S. 6,889,242).

Re claim 1, Sijstermans et al. disclose in Figures 1-2 and 4 a method for averaging two pixel values (e.g. abstract, Figure 4, and claim 2 in col. 15), comprising:

decoding a single machine code instruction (e.g. component18 in Figure 1) comprising an address for a first input register, an address for a second input register, an address for an output register (e.g. col. 3 lines 45-53), an op code indicating a function to perform (e.g. as a functional code by unit 14 in Figure 1 and col. 3 lines 45-66), and a rounding factor (e.g. component 202 in Figure 2 and col. 4 line 55 to col. 5 line 45);

loading a plurality of first operands from a first input register (e.g. rsrc1 as vectors in col. 6 lines 40-50);

loading a plurality of second operands from a second input register (e.g. rsrc2 as vectors in col. 6 lines 40-50);

producing an average, based on the op code, of one of the plurality of first operands and one of the plurality of second operands (e.g. output of Figure 4 after the right shifting and claims 1-2 in col. 15), wherein the rounding factor indicates which of a plurality of rounding algorithms to use in producing the average (e.g. col. 6 lines 55-65 and table 1 in col. 5), the plurality of rounding algorithms comprising:

a first rounding algorithm able to produce a change in the average (e.g. depending on the rounding mode as seen in col. 5 lines 1-15); and

a second rounding algorithm able to produce a change in the average (e.g. depending on the rounding mode as seen in col. 5 lines 1-15); and storing the average in an output register (e.g. rdest as vectors in col. 6 lines 40-50).

Re claim 2, Sijstermans et al. further disclose in Figures 1-2 and 4 determining how many fields are in each of the first and second input registers (e.g. col. 5 line 65 to col. 6 lines 55).

Re claim 3, Sijstermans et al. further disclose in Figures 1-2 and 4 the producing the average comprises: producing a first intermediate result by adding one of the plurality of first operands to one of the plurality of second operands (e.g. component 402 in Figure 4); and producing the average by shifting the first intermediate result to the right by one binary digit (e.g. component 404 in Figure 4).

Re claim 4, Sijstermans et al. further disclose in Figures 1-2 and 4 the producing the average comprises: producing a first intermediate result by adding one of the plurality of first operands, one of the plurality of second operands and the rounding factor (e.g. 402 and 406 in Figure 4); and producing the average by shifting the first intermediate result to the right by one binary digit (e.g. component 404 in Figure 4).

Re claim 5, Sijstermans et al. further disclose in Figures 1-2 and 4 rounding the average before storing the average (e.g. rounding in components 402-404 before output the results as rdest).

Re claim 6, Sijstermans et al. further disclose in Figures 1-2 and 4 evaluating the rounding factor, and adding a value to the average (e.g. col. 1 lines 1-45 and particularly table 1).

Re claim 7, Sijstermans et al. further disclose in Figures 1-2 and 4 the value is one of zero and one (e.g. component 406 in Figure 4 and col. 5 lines 1-45).

Re claim 8, it is a method claim having similar limitations cited in claim 1. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 9, Sijstermans et al. further disclose in Figures 1-2 and 4 the instruction is one of a plurality of instructions in a long instruction word (e.g. col. 6 line 47 as VLIW).

Re claim 10, it is a method claim having similar limitations cited in claim 2. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 11, it is a method claim having similar limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it is a method claim having similar limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it is a method claim having similar limitations cited in claim 6. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 14, it is a method claim having similar limitations cited in claim 7. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 15, Sijstermans et al. further disclose in Figures 1-4 the first input register comprises a plurality of fields (e.g. Figure 3 wherein vector is a set of plurality of elements).

Re claim 16, it is a method claim having similar limitations cited in claim 5. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 17, Sijstermans et al. further disclose in Figures 1-2 and 4 loading a third operand from an A2 field of the first input register; loading a fourth operand from a B2 field of the second input register; producing a second average of the third operand and the fourth operand, and storing the second average in a C2 field of the output register (e.g. additional process of averaging step as seen in Figure 4 and col. 6 line 40 to col. 7 line 15).

Re claim 18, it is an apparatus claim having similar limitations cited in claim 1. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 19, Sijstermans et al. further disclose in Figures 1-2 and 4 average module comprises: a plurality of adders respectively coupled to the first and second fields (e.g. inherently for adding vectors as seen in Figure 4); and a plurality of shifters respectively coupled to the plurality of adders (e.g. inherently for shifting vectors as seen in Figure 4).

Re claim 20, Sijstermans et al. further disclose in Figures 1-2 and 4 the rounding factor causes at least one of rounding-up or rounding-down by the plurality of average modules (e.g. col. 5 lines 1-15).

Re claim 21, Sijstermans et al. further disclose in Figures 1-2 and 4 the rounding factor is added to the first and second fields in the average module (e.g. component 406 in Figure 4 and col. 5 lines 1-45).

(10) Response to Argument

A. Discussion of the rejection of only independent method claims 1 and 8 under 35 U.S.C. § 102(e) as being anticipated by Sijstermans et al. (U.S. 6,889,242).

The applicant mainly argues in page 7 second paragraph for claims 1 and 8 that the cited reference by Sijstermans et al. fail to disclose an operation of decoding a single machine code instruction comprising an address for a first input register, an address for a second input register, and address for an output register, an op code indicating a function to perform, and a rounding factor as cited in the claimed invention.

The examiner respectfully submits that the rejection above clearly addresses how the cited reference by Sijstermans et al. either individual or combine of expressively and inherently meet every limitations cited in the claim. In particular, Sijstermans et al. disclose an decoded-able instruction as a VLIW instruction capable of including a multiple instruction slots wherein each slot may be adapted to executed one operation (e.g. col. 3 lines 55-68). The reference clearly discloses VLIW instruction comprising addresses of source and destination for fetching and storing the operands (e.g. col. 3 lines 45-53 and col. 6 lines 1-40); an op-code indicating function to perform wherein the function in this case is the average function as seen in an example in column 6 lines 1-40; and a rounding factor which can be executed according to the control register 22 (e.g. col.

3 lines 45-53). In general, the VLIW instruction is known in the art of technology as a single instruction having multiple sub-instructions for efficiently executed or decoded to perform at least a plurality of instructions.

The applicant argues in page 7 third paragraph in response to the basis set forth in the final Office Action that the cited reference by Sijstermans et al. do not sufficiently provide a basis for anticipation of decoding a single machine code instruction as cited in the claimed invention.

The examiner respectfully submits that Figure 1 of the cited reference by Sijstermans et al. clearly provide the basis of decoding the single machine code instruction as cited in the claimed invention wherein the decoder unit 18 in Figure 1 is excuted to decode the instruction provided and controlled by the control unit 12.

The applicant argues in page 7 fourth and fifth paragraphs for claims 1 and 8 that the cited reference by Sijstermans et al. fail to provide a rounding factor in the decoded instruction as cited in the claimed invention.

As previously mentioned by the examiner in the above responses, the rounding factor is provided in the instruction in order to execute properly as clearly stated in column 2 lines 31-49, col. 3 lines 45-55, and col. 12 lines 45-57. After a specific function is performed, a rounding term is added to the result according to the rounding mode.

Further, the applicant argues in page 8 first paragraph for claims 1 and 8 that the cited reference by Sijstermans et al. fail to show or teach the VLIW instruction include the rounding factor along with other fields as input and output register and an opcode as cited in the claimed invention.

The examiner respectfully submits that a detail of VLIW instruction is cited in column 3 line 54 to column 4 line 22 which clearly discloses that a VLIW instruction is a single instruction comprising multiple sub-instructions for performing multiple functions corresponding to the sub-instructions having an input and output registers (e.g. col. 3 lines 35-44 for fetching source data and storing destination data); an opcode (e.g. example of functions in col. 3 lines 1-9); and a rounding factors (e.g. as addressed above wherein the rounding factor is included with the instruction in order to perform rounding correctly according to the user's specific in column 2 lines 31-49, col. 3 lines 45-55, and col. 12 lines 45-57).

The applicant argues in page 8 second paragraph for claims 1 and 8 that the cited reference by Sijstermans et al. disclose the rounding factor is set in a separate instruction from the opcode instruction wherein the invented instruction comprising the rounding factor with the opcode and input and output register addresses.

The examiner respectfully submits that the VLIW instruction is a single instruction capable of packing multiple instructions together for efficiently executing. Thus, the VLIW instruction is a single instruction having multiple sub-instructions including the average and rounding sub-instructions together as a single instruction.

Further, the applicant argues in page 8 last paragraph to page 9 first paragraph that the cited reference by Sijstermans et al. discloses two separate instructions wherein the first instruction for setting or designating a rounding factor and the second instruction for performing an arithmetic function/operation. Unlike the claimed invention, it has only one instruction which comprising: an input and output addresses, an opcode, and a rounding factor.

The examiner respectfully submits that the VLIW instruction is well-known in the art of technology for executing multiple instruction in a single instruction. Thus, the VLIW instruction is capable of designating two separate instructions as single VLIW instruction wherein the first instruction for setting or designating a rounding factor and the second instruction for performing an arithmetic function/operation.

B. Discussion of the rejection of only independent apparatus claim 18 under 35 U.S.C. § 102(e) as being anticipated by Sijstermans et al. (U.S. 6,889,242).

The applicant argues in page 9 last paragraph for claim 18 that the cited reference by Sijstermans et al. fail to disclose a plurality of average modules configured to perform an averaging function indicated by an opcode in the single machine code instruction as cited in the claimed in addition to the missing features as argued repeatedly above.

In addition to the above responses, the examiner respectfully submits that the cited reference by Sijstermans et al. also disclose a plurality of average modules to

perform an averaging function in Figure 3 wherein each of average operation done on an element of operand (e.g. see col. 6 lines 25-45) corresponding to an average module. An example is seen in col. 6 lines 25-45 in which an average operation is performed in a set of four elements of operands as vector.

The applicant argues in page 10 second paragraph for claim 18 that the examiner fails to set forth a proper basis for rejection by asserting that claim 18 "is an apparatus claim of claim 1. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 1".

The examiner respectfully submits that even claim 18 has slightly different wording compares to method claims 1 and 8. However, the context of claim 18 is the same as context of claims 1 and 8. In another words, claim 18 either expressively or inherently has similar features or limitations cited in the method claims 1 or 8. Therefore, it is proper to conclude that claim 18 can be rejected under same rationale as cited in the rejection of rejected claims 1 or 8.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Chat C. Do

AU 2193

09/10/2007

Conferees:

Meng-Ai An

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Eddie Lee

EDDIE C. LEE
SUPERVISORY PATENT EXAMINER